REMARKS

SUMMARY OF THE OFFICE ACTION

Drawings 1-6 stand objected to because the top margins are not acceptable and the lines, numbers and letters are not uniformly thick and well defined, clean, durable and/or black.

Claims 1-4, 8-12 and 21 stand rejected under 35 USC §103(a) as being unpatentable over *Berger* (US Patent No. 4,679,166) in view of *Mills* (US Patent No. 6,026,465). Claims 5-6, 13-14 and 19-20 stand rejected under 35 USC §103 as being unpatentable over *Berger* and *Mills* in view of *Stapleton* (US Patent No. 6,106,565). Claims 7 and 15 stand rejected under 35 USC §103 as being unpatentable over *Berger* and *Mills* in further view of *Jaff* (US Patent No. 5,384,692). Claims 16 and 18 stand rejected under 35 USC §103 as being unpatentable over *Berger* and *Mills* in view of *Youens* (US Patent No. 6,058,089). Claim 17 stands rejected under 35 USC §103 as being unpatentable over *Berger*, *Mills*, and *Youens*, in further view of *Jaff* (US Patent No. 5,384,692).

SUMMARY OF THE RESPONSE

Claims 1, 3-4, 8, 11, 12, 16 and 18 have been once amended, and claim 21 has been cancelled without prejudice leaving claims 1-20 pending for examination.

OBJECTION TO DRAWINGS

Applicants have amended Figures 1-6 to correct informalities noted by Examiner. Applicants submit that no new matter has been added. Two copies of Amended Figures 1-6 are included herewith under separate cover for Examiner's approval.

REJECTIONS TO CLAIMS 1-4, 8-12 AND 21 RELYING ON *BERGER* AND *MILLS*

Applicants' amended claim 1 is directed to an apparatus comprising:

> a first plurality of electronic components defining an instant on mode of operation;
> a second plurality of electronic components defining a non-instant on mode of operation;
> a plurality of input/output devices; and
> one or more switching mechanisms to selectively couple one or more of said plurality of input/output devices to one or more of said first plurality of electronic components and enable said apparatus to start up in said instant on mode of operation to the exclusion of said second plurality of electronic components, or to selectively couple said one or more input/output devices to one or more of said second plurality of electronic components and enable said apparatus to start up in said non-instant on mode of operation to the exclusion of said first plurality of electronic components.

Thus in accordance with amended claim 1, the apparatus can operate in a first instant on mode of operation, which uses one set of electronic components and one or more of a set of input/output devices, or a second non-instant on mode of operation, which uses a second set of electronic components and one or more of the previously mentioned set of input/output devices. Accordingly, a user may avoid a lengthy start up process and conserve power by choosing to have the apparatus directly start up in an instant on mode, while still having access to input/output devices such as a full-size keyboard, display, mouse and

so forth, typically reserved for use within a non-instant on mode of operation. On the other hand, if a user desired the full range of functionality offered by the non-instant on mode of operation, the user may alternatively choose to have the apparatus directly start up in a non-instant on mode of operation without first starting in the instant on mode of operation.

Berger however, is directed to a co-processor combination including both an 8-bit processor and a 16-bit processor for providing backwards compatibility between two operating systems. When in 16-bit operation, one of the processors (e.g. 8-bit) is dedicated to input/output tasks while the other (e.g. 16-bit) is dedicated to high level language tasks. More specifically, the boot-up procedure described in *Berger* forces the 8-bit processor to turn on first to "thus initially make the system appear as an 8-bit system." This is said to "have the advantage of making the usual 16-bit machine compatible with 8-bit software written for an 8-bit machine even though the system is normally operated as a 16-bit machine." *(emphasis added; See Col. 1, lines 9-38 & Col. 2 lines 1-28).* Thus, regardless of the type of operating system used in *Berger* (i.e. 8-bit or 16-bit), one processor (8-bit) always turns on first so that the system initially appears as an 8-bit system. If the software consists of an 16-bit operating system, the 16-bit processor is enabled by the 8-bit processor, which then functions as an I/O processor. Therefore, operation of the 16-bit processor is dependent upon the state of the 8-bit processor. Furthermore, when the system operates as a 16-bit system, both the 16-bit and 8-bit processors are concurrently utilized further increasing the power requirements of the system.

Applicants submit that *Berger* does not teach a first plurality of electronic components defining an instant on computing device, let alone a system having selectable modes of independent operation including a first instant on operating mode and a second non-instant on operating mode. Even if one were to assume that the 8-bit processor of *Berger* could be analogized to the plurality of electronic components defining an instant on mode of operation in claim 1, and the 16-bit processor of *Berger* could be analogized to the second plurality of electronic components defining a non-instant on mode of operation, the operation of the 16-bit processor nonetheless explicitly depends upon the concurrent operation of the 8-bit processor where it does not in claim 1.

Mills teaches a flash memory including a mode register for indicating synchronous or asynchronous operation. The present Office Action states that *Mills* discloses an apparatus comprising a first plurality of electronic components defining an instant on computing device for use in a first instant on mode of operation. Whether or not *Mills* teaches that which it is purported to teach, Applicants respectfully submit that *Mills* does not teach one or more switching mechanisms to selectively couple one or more of a plurality of input/output devices to one or more of a first plurality of electronic components and enable an apparatus to start up in said instant on mode of operation to the exclusion of a second plurality of electronic components, or to selectively couple the one or more input/output devices to one or more of the second plurality of electronic components and enable the apparatus to start up in a non-instant on mode of operation to the exclusion of the first plurality of electronic components.

The present Office Action states that it would have been obvious to include *Mill's* instant on feature with the non-instant on feature of *Berger* because both *Berger* and *Mills* use two processors. Applicants submit that even if *Mills* could be said to teach an instant on feature (which Applicants maintain is not the case), it would not have been obvious to one of ordinary skill in the art to combine such teachings with the *Berger* reference. More specifically, *Berger* is directed to maintaining backwards compatibility between 8-bit and 16-bit operating systems. By combining instant on functionality with the teachings of the *Berger* system, the goals of achieving backwards compatibility would be hindered due to the additional instant on functionality not present in the previous operating systems.

Accordingly, for at least the reasons set forth above, Applicants submit that claim 1 is patentable over *Berger* in view of *Mills*. Since, independent claim 8 includes limitations similar to those of independent claim 1, Applicants submit that independent claim 8 is likewise patentable over *Berger* in view of *Mills*.

REJECTIONS TO CLAIMS 2-4 & 9-12 RELYING ON *BERGER* AND *MILLS* IN VIEW OF VARIOUS COMBINATIONS OF *STAPLETON & JAFF*

Applicants submit that by virtue of at least their dependency on claims 1 and 8, claims 2-7 and 9-15 respectively, are likewise patentable over *Berger* in view of *Mills* as well as *Berger* and *Mills* in view of various combinations of Stapleton & Jaff.

REJECTIONS TO CLAIMS 16 AND 18 RELYING ON *BERGER* AND *MILLS* IN VIEW OF YOUENS

Independent claim 16 includes limitations similar to those of claims 1 and 8. Therefore, for at least the reasons set forth above, Applicants submit that claim 16 is similarly patentable over *Berger* in view of *Mills*. Whether or not Youens teaches that which it is cited as teaching, *Youens* does not cure the above-discussed deficiencies of *Berger* and/or *Mills* and thus, even when the three references are combined, claim 16 remains patentable over them.

Applicants further submit that by virtue of at least their dependency on claim 16, claims 17-20 are also patentable over *Berger* in view of *Mills* as well as *Berger* and *Mills* in view of various combinations of *Youens*, *Stapleton* & *Jaff*.

CONCLUSION

In view of the foregoing, Applicants submit that claims 1-20 are in condition for allowance and early issuance of the Notice of Allowance is respectfully requested.

Respectfully submitted,

COLUMBIA IP LAW GROUP, PC

Date: 1/4 by: _____

Jason K. Klindtworth
Reg. No. 47,211

10260 SW Greenburg Rd.
Suite 820
Portland, OR 97223
Phone: (503) 595-2800

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Amended) An apparatus comprising:

a first plurality of electronic components defining an instant on ~~computing device for use in a first instant on~~ mode of operation;

a second plurality of electronic components~~, including a plurality of input and output devices~~ defining a non-instant on ~~computing device for use in a second non-instant on~~ mode of operation; ~~and~~

a plurality of input/output devices; and

one or more switching mechanisms to selectively couple one or more of said plurality of input/output devices ~~coupled~~ to ~~said input and output devices and selectively, to selected ones of~~ one or more of said first ~~and second~~ plurality of electronic components ~~to~~ and enable said apparatus to start up ~~input/output devices to be available for use~~ in said ~~first~~ instant on ~~as well as said second non-instant on~~ mode of operation to the exclusion of said second plurality of electronic components, or to selectively couple said one or more input/output devices to one or more of said second plurality of electronic components and enable said apparatus to start up in said non-instant on mode of operation to the exclusion of said first plurality of electronic components.

3. (Amended) The apparatus of claim 2, wherein said first plurality of electronic components includes a first memory device and said second plurality of electronic components includes a second memory device, and wherein after start up said first and second processors operate simultaneously to synchronize data between said first and second memory devices.

4. (Amended) The apparatus of claim 1, wherein at least one of said first ~~or~~ and second plurality of electronic components includes a processor having at least two operating modes, wherein when in a first operating mode said processor executes instructions representing a first operating system, and when in a second operating mode said processor executes instructions representing a second operating system.

8. (Amended) An apparatus comprising:

an integrated circuit having a plurality of function blocks for use in a first instant on mode of operation;

a plurality of electronic components~~, including a plurality of input and output devices, said plurality of electronic components~~ for use in a second non-instant on mode of operation; ~~and~~

a plurality of input and output devices; and

one or more switching mechanisms to selectively coupled ~~to~~ one or more of said plurality of input and output devices ~~and selectively, to selected~~ ones or more of said function blocks ~~and said plurality of electronic components~~ to enable said one or more ~~said~~ input and output devices to be available for use in said first instant on ~~as well as~~

~~said second non-instant on~~ mode of operation to the exclusion of said a plurality of electronic components, or to selectively couple said one or more of said plurality of input and output devices to one or more of said plurality of electronic components to enable said one or more input and output devices to be available for use in said second non-instant on mode of operation to the exclusion of said plurality of function blocks.

11. (Amended) The apparatus of claim 9, wherein said plurality of function blocks includes a first memory device, wherein said second plurality of electronic components includes a second memory device, and wherein after start up said first and second processors operate simultaneously to synchronize data stored within said first and second memory devices.

12. (Amended) The apparatus of claim 8, wherein at least one of said plurality of function blocks and ~~or~~ said plurality of electronic components include a processor having at least two operating modes, wherein when in a first operating mode, said processor executes instructions representing a first operating system, and when in a second operating mode, said processor executes instructions representing a second operating system.

16. (Amended) An integrated circuit comprising:

a first processor block to operate in a first instant on mode of operation;

a second processor block to operate in a second non-instant on mode of operation; ~~and~~

a plurality of input/output ports; and

one or more switching mechanisms ~~coupled~~ to selectively couple one or more external devices to~~, to selected ones of~~ said first ~~and second~~ processor blocks through at least one of said plurality of input/output ports to ~~enable~~ facilitate use of said one or more external devices in said instant on mode of operation to the exclusion of said second processor block, or to selectively couple said one or more external devices to said second processor block through at least one of said plurality of input/output ports to facilitate use of said one or more external devices in said non instant on mode of operation to the exclusion of said first processor block~~data routing between said selected ones of said first and second processor blocks and a plurality of external devices~~.

18. (Amended) The integrated circuit of claim 16, wherein said plurality of external devices includes a first memory device and a second memory device, and wherein after start up said first and second processor blocks operate simultaneously to synchronize data between said first and second memory devices.